CLAIMS

1. A method of forming a transistor in a semiconductor active area, comprising the steps of:

forming a gate structure in a fixed relationship to the semiconductor active area and comprising a first sidewall and a second sidewall and thereby defining a first source/drain region adjacent the first sidewall and a second source/drain region adjacent the second sidewall; and

forming a lightly doped diffused region formed in the first source/drain region and extending under the gate structure, comprising the step of forming the lightly doped diffused region to comprise a varying resistance in a direction parallel to the gate structure.

2. The method of claim 1 wherein the step of forming a lightly doped diffused region comprises:

selectively masking the first source/drain region such that a portion of the first source/drain region is covered and a portion of the first source/drain region is exposed; and

during the selectively masking step, directing dopants toward the first source/drain region.

3. The method of claim 2 wherein as a result of the directing step a first concentration of dopants are implanted in the portion of the first source/drain region that is exposed while a different concentration of dopants are implanted in the portion of the first source/drain region that is covered, wherein the first concentration is greater than the different concentration.

4. The method of claim 2:

wherein the step of selectively masking comprises a first selectively masking step performed using a mask; and

wherein the mask comprises a plurality of elements such that the portion of the first source/drain region that is covered is covered by the plurality of elements and such that the portion of the first source/drain region that is exposed is not covered by the plurality of elements.

5. The method of claim 4 wherein each element of the plurality of elements spans in a direction perpendicular to the gate structure and has a same first distance length in a direction along the gate structure.

6. The method of claim 5 wherein each element of the plurality of elements has a same second distance length, along the gate structure, between itself and an adjacent other one of the plurality of elements.

7. The method of claim 6 wherein the first same distance length equals the same second distance length.

8. The method of claim 2:

wherein the transistor is formed as part of an integrated circuit comprising input/output circuitry and core circuitry; and

wherein the transistor is formed as part of the input/output circuitry.

9. The method of claim 8:

wherein the transistor comprises a first transistor in a first plurality of transistors;

wherein the step of selectively masking selectively masks a respective first source/drain for each transistor in the first plurality of transistors; and

wherein the step of directing dopants directs dopants toward a respective first source/drain for each transistor in the first plurality of transistors.

10. The method of claim 9 wherein each transistor of the first plurality of transistors is formed as part of the input/output circuitry.

11. The method of claim 8 wherein the transistor comprises a first transistor, and further comprising forming a second transistor in the core circuitry, wherein the step of directing dopants further directs dopants into a first source/drain and a second source/drain of the second transistor.

12. The method of claim 11:

wherein the step of selectively masking comprises selectively masking using a mask; and

wherein the active area of the second transistor is not masked by the mask.

13. The method of claim 2 wherein the step of directing dopants comprises directing n-type dopants.

14. The method of claim 2 wherein the step of directing dopants comprises directing p-type dopants.

15. The method of claim 2:

wherein the step of selectively masking comprises selectively masking using a mask; and

wherein the second source/drain is not masked by the mask.

16. The method of claim 2:

wherein the step of selectively masking comprises a first selectively masking step performed using a mask;

and further comprising, at the same time as the first selectively masking step, the step of using the mask for second selectively masking the second source/drain region such that a portion of the second source/drain region is covered and a portion of the second source/drain region is exposed;

and wherein the step of directing dopants further comprises directing dopants toward the second source/drain region.

17. The method of claim 16 wherein as a result of the directing step a first concentration of dopants are implanted in the portion of the first source/drain region that is exposed and the second source/drain that is exposed while a different concentration of dopants are implanted in the portion of the first source/drain region that is covered and the portion of the second source/drain region that is covered, wherein the first concentration is greater than the different concentration.

18. The method of claim 17:

wherein the step of selectively masking comprises a first selectively masking step performed using a mask; and

wherein the mask comprises a plurality of elements such that the portion of the first source/drain region that is covered and the portion of the second source/drain region that is covered are covered by the plurality of elements and such that the portion of the first source/drain region that is exposed and the portion of the second source/drain region that is exposed are not covered by the plurality of elements.

19. The method of claim 18 wherein each element of the plurality of elements spans in a direction perpendicular to the gate structure and has a same first distance length in a direction along the gate structure.

20. The method of claim 19 wherein each element of the plurality of elements has a same second distance length, along the gate structure, between itself and an adjacent other one of the plurality of elements.

21. The method of claim 20 wherein the first same distance length equals the same second distance length.

22. The method of claim 17:

wherein the transistor is formed as part of an integrated circuit comprising input/output circuitry and core circuitry; and

wherein the transistor is formed as part of the input/output circuitry.

23. The method of claim 22:

wherein the transistor comprises a first transistor in a first plurality of transistors;

wherein the step of selectively masking selectively masks a respective first source/drain and a respective second source/drain for each transistor in the first plurality of transistors; and

wherein the step of directing dopants directs dopants toward a respective first source/drain for each transistor in the first plurality of transistors and a respective second source/drain for each transistor in the first plurality of transistors.

24. The method of claim 17 wherein the step of directing dopants comprises directing n-type dopants.

25. The method of claim 17 wherein the step of directing dopants comprises directing p-type dopants.

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the varying resistance occurs between areas having LDD and areas without LDD. there is no varying resistance within a given LDD region.

102 - FIG. 1
2002/0019104

102 - FIG. 5, ¶[0039] says only input protection circuit (504) and output transistor (505) are non-LDD. the rest (e.g. input-output transistor (506) would have the LDD structure of inverter.

102 - FIG. 4 shows LDD on source side also.

26. An integrated circuit comprising a transistor, the transistor comprising:

a gate structure in a fixed relationship to a semiconductor active area and comprising a first sidewall and a second sidewall and thereby defining a first source/drain region adjacent the first sidewall and a second source/drain region adjacent the second sidewall; and

a lightly doped diffused region formed in the first source/drain region and extending under the gate structure, wherein the lightly doped diffused region comprises a varying resistance in a direction parallel to the gate structure.

27. The integrated circuit of claim 26:

wherein the integrated circuit further comprises input/output circuitry and core circuitry; and

wherein the transistor is formed as part of the input/output circuitry.

28. The integrated circuit of claim 26:

wherein the integrated circuit further comprises a first plurality of transistors;

wherein the transistor comprises a first transistor in the first plurality of transistors;

wherein each transistor of the plurality of transistors comprises:

a gate structure in a fixed relationship to a semiconductor active area and comprising a first sidewall and a second sidewall and thereby defining a first source/drain region adjacent the first sidewall and a second source/drain region adjacent the second sidewall; and

a lightly doped diffused region formed in the first source/drain region and extending under the gate structure, wherein the lightly doped diffused region comprises a varying resistance in a direction parallel to the gate structure.

102 (see claim 27)

29. The integrated circuit of claim 28:

wherein the integrated circuit further comprises input/output circuitry and core circuitry; and

wherein the plurality of transistors are formed as part of the input/output circuitry.

102 FIGH along LDD on both source & drain sides

30. The integrated circuit of claim 28 wherein each transistor of the plurality of transistors further comprises a lightly doped diffused region formed in the second source/drain region and extending under the gate structure, wherein the lightly doped diffused region formed in the second source/drain region comprises a varying resistance in a direction parallel to the gate structure.

102 See claim 27

31. The integrated circuit of claim 28:

wherein the integrated circuit further comprises input/output circuitry and core circuitry; and

wherein the plurality of transistors are formed as part of the input/output circuitry.

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